transistor has a gate electrode and first and second electrodes defining a serpentine channel region there between voltage applied to the gate electrode controls conductivity of the channel region. Preferably, a common electrode includes one of the first and second electrodes of the first transistor and one of the first and second electrodes of the second transistor. The first and second transistors are preferably coupled between a gate line (or data line) and respective probe pads formed on the substrate and selectively couple the respective probe pad to the gate line (or data line) during a test routine whereby charge is written to, stored, and read from the array of pixel cells.

IN THE DRAWINGS:

The Examiner is requested to review and approve the proposed changes to Fig. 2 and Fig. 3 in the attached Submission of Proposed Drawing Corrections.

IN THE CLAIMS:

Please add claims 7 - 20 as follows:

- - 7. (Newly Added) The system of claim 1, wherein said first transistor comprises a select transistor and is connected to a first probe pad and a gate select control pad and wherein said second transistor comprises a hold transistor and is connected to a second probe pad and a gate hold control pad. - -

- - 8. (Newly Added) The system of claim 7, wherein said select transistor and said hold transistor are connected by a common electrode to at least one of said plurality of gate lines. - -